

Cognovo SDM Development Platform

Rapid, Real-time Modem Design and Verification

The Cognovo SDM Development Platform (CDP) provides a real-time platform on which to develop and run Software Defined Modems for interoperability and power/performance verification against industry standard test equipment and networks.



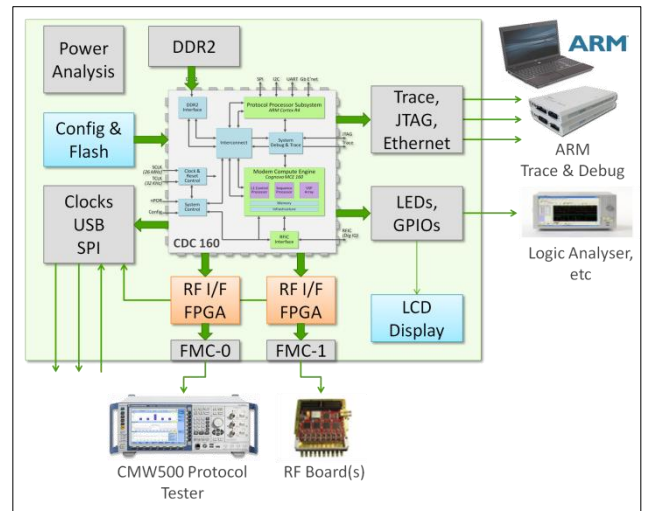
CDP with Rohde & Schwarz CMW500

The CDP is built around Cognovo's CDC160 development chip which includes a Modem Compute Engine (MCE) with 6 Vector Signal Processor (VSP) cores; an ARM Cortex R4 CPU; dual Turbo Decoders; and a multi-channel IQ interface to support radios. CDC160 also features a second ARM Cortex R4 Protocol Stack CPU with external I/O for debug and trace and a Gbit/s data interface, allowing full modem and protocol stack development and integration. Operating at 300MHz, the device achieves an unprecedented 120GMAC/s (250Gops/s) of performance at low power.

Key Features

- Supports real-time development and validation for all wireless standards
- Software Defined Modem IC (CDC160)
- Fully code compatible with MCE system model for rapid software integration

- Fully integrated with ARM code development suite and Coresight debug & trace tool chain
- Programmable FPGA interface supports integration with MIMO, multi-carrier and multi-mode RFIC designs with multi-sourced clocks and PLL settings
- System Controller covering 35 Power Domains and Deep Sleep Power down



CDP System Configuration

Supported Interfaces

- ARM Coresight (JTAG & Trace) 300MByte/s interface to ARM IDE and Cognovo Event Viewer (Evi):
 - 2x CPU ETM and System Level Trace (STM)
 - Performance and Memory Watch traces
- 200MHz 128Mbyte 32bit DDR2 memory
- Gigabit Ethernet Interface to host PC
- USB to PC for higher layer test software, or additional software debug interface
- Digital I/Q Interface:
 - 2x 32bit Parallel 80MHz LVDS channels
 - Supports up to 4 RX and 2 TX Antennas
 - Supports Rohde and Schwarz EX-IQ capable test equipment, such as the CMW500 Communication Tester
 - TX > RX Loopback mode
- 5x SPI for RF, PMIC Control and general I/O
- I²C
- GPIO Port for software debug and control

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CDC160 Features

- 6 VSP cores
- 2 Programmable Turbo FEC engines
- HARQ RAM buffer
- 300MHz ARM R4 based Layer 1 control plane
- Programmable time base and slow clocking
- PHY Sequence Processor
- Standard ARM infrastructure components
 - ARM GIC, SDMA, WDT, Timers, Coresight
- CDC160 memory configuration shown below:

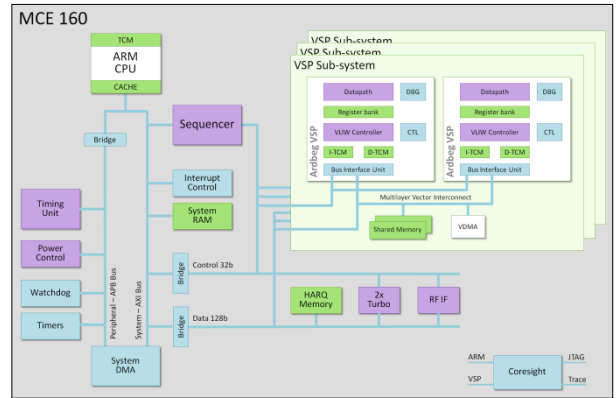
VSP	I-TCM (x6)	64 kB
	D-TCM (x6)	64 kB
	Shared RAM (x3)	512 kB
ARM L1	A-TCM	128 kB
	B-TCM	128 kB
	I-Cache	16 kB
	D-Cache	16 kB
System RAM		256 kB
HARQ RAM Buffer		256 kB
ARM L23	A-TCM	128 kB
	B-TCM	128 kB
	I-Cache	16 kB
	D-Cache	16 kB

CDC160 Memory Configuration

Modem Compute Engine

The MCE family includes a hardware sequencer engine which ensures that all VSP code execution is managed with clock cycle precision to provide deterministic, real time, access to the high performance PHY processing resources, leaving the ARM Cortex R4 processor focussed on Layer 1 control. A full multi-mode time-base engine with slow clocking, and a Turbo Decoder supporting 3GPP and WiMAX standards, coupled to a high bandwidth AMBA AXI infrastructure and HARQ cache completes the platform.

Extensive power domain control delivers system level power consumption which matches or betters that achieved by the current hardware modem designs deployed in mobile handsets today.



Modem Compute Engine System Overview

SDM Design Flow

A key benefit of the Software Defined Modem approach is that Layer 1 control, Sub-frame sequencing and Physical Layer signal processing are all developed in software in parallel.

Cognovo's Integrated Development Environment allows optimised development and validation of Physical Layer signal-processing kernels using the **Kernel SDK** together with system integration, constraint optimisation and verification of the overall modem using the **System SDK**.

Once the modem software has been integrated and tested in simulation, the complete modem, including the RF sub-systems can be fully validated in real time, with cycle precise operation, against standard test equipment using the CDP. Performance against reference simulations can be fully verified and optimised while production silicon is under development and fabrication.

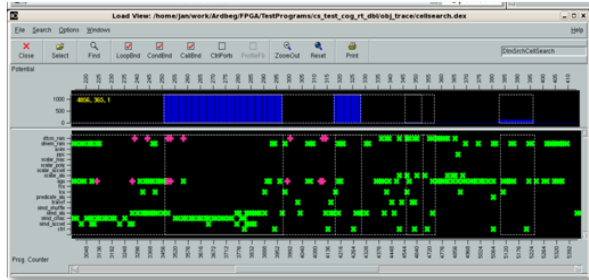
Kernel SDK Overview

The Kernel SDK enables efficient creation of Physical Layer software to run on the VSPs. Based entirely in C with the use of ISA intrinsics, the design flow enables vectorisation to be validated entirely within existing link level simulation environments, before targeting the Vector Signal Processor. At any time during subsequent optimisation the original test vectors and

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simulation environment can be re-used. The Kernel SDK comprises:

- ISA Integration with Link Level simulations
- VSP Parallelising C compiler
- Cycle Accurate Instruction Set Simulator
- Performance profiler and analysis tool
- VSP Maths Library and LTE PHY Library.

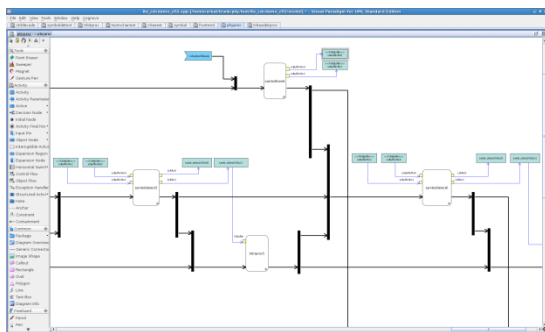


Kernel SDK : Profiler and Analysis Tool

From initial algorithm selection, right through to target C-code optimisation, key metrics are recorded in the Kernel Library for use in the System SDK during top-down PHY development.

System SDK Overview

The System SDK enables rapid Layer 1 / PHY system integration and validation. The PHY partitioning, Kernel APIs, control and data flows can be compiled and analysed via the System Design Tool and simulated in the MCE System Model. A simple build configuration maps the Layer 1 / PHY design to the CDP for full verification against test peers and RF systems, using the Cognovo trace viewer for both hardware and software events.



System SDK : PHY System Design Capture

The System SDK comprises:

- System Design Tool for PHY sequencing and control / data flow optimisation
- MCE System Model for Layer 1 integration and validation
- Trace decoder and Event Viewer (Evi) for non-intrusive debug and performance verification.

The Cognovo SDM Development Platform

The package comprises:

- One CDP System Board
 - Physical size: 24 cm (L) x 25 cm (W)
 - R&S EXIQ compliant I/F card (4Rx, 2Tx)
 - Power supply and interface cables
- Run-time SDMOS and example application software:
 - Simple initialisation and control example
 - LTE downlink example
- Development Environment
 - System SDK and Kernel SDK
- Full Documentation
- Training courses on the use of the platform and development environment
- Technical Support
- Also required and available from ARM:
 - RealView Development Suite (RVDS) or DS:5
 - DStream JTAG and Trace Acquisition pod.

Next Steps

The Cognovo SDM-DP is the perfect platform for development of multi-mode modems using Software Defined Modem techniques. It allows you to develop and test a complete modem in parallel with the development of your own silicon.

Contact Cognovo for pricing and availability.